WHAT IS CLAIMED IS:

1. A unified serial link system comprising a transmitter portion and a receiver portion, one of said transmitter portion and said receiver portion further comprising

a. a phase locked loop control circuit;

b. a phase rotator circuit connected to the phase locked loop control circuit;

c. a phase buffer circuit connected to the phase rotator circuit; and

d. an equalization driver circuit connected to said phase buffer circuit;

wherein the phase rotator circuit is configured to acquire a clock phase from the phase locked loop control circuit and modulo shift the clock phase into a desired phase angle.

2. The unified serial link system of claim 1 wherein the phase locked loop control circuit further comprises a first loop, said first loop comprising:

a. a voltage control oscillator connected to the phase rotator circuit and configured to receive a coarse control voltage signal and a fine control voltage signal and generate the clock phase to the phase rotator and a voltage control oscillator signal;

b. a frequency divider connected to the voltage control oscillator to receive the voltage control oscillator signal, the frequency divider configured to generate a frequency divider output;

c. a phase-frequency detector connected to the frequency divider and configured to receive the frequency divider output and generate a phase-frequency detector output;

d. a charge pump connected to the phase-frequency detector and configured to receive the phase-frequency detector output and generate a charge pump output; and

e. a multi-pole loop filter connected to the charge pump and the voltage control oscillator, the multi-pole loop filter configured to receive the

charge pump output and generate the fine control voltage signal to the voltage control oscillator.

3. The unified serial link system of claim 2 wherein the phase locked loop control circuit further comprises a second loop, said second loop comprising:

a. a voltage comparator connected to the multi-pole loop filter and configured to receive the fine control voltage signal;

b. a reference generator connected to the voltage comparator and configured to generate a reference signal; wherein said voltage comparator generates a comparator output from the fine control voltage signal and the reference signal;

c. a phase locked loop control logic circuit connected to the comparator configured to sample the comparator output and generate a control logic output;

d. a digital to analog converter connected to the phase locked loop control logic circuit and configured to receive the control logic output and generate a control voltage output;

e. a low pass filter connected to the digital to analog converter and to the voltage control oscillator and configured to receive the control voltage output and generate the coarse control voltage signal.

4. The unified serial link system of claim 3 wherein the voltage control oscillator is a dual-delay voltage controlled oscillator comprising negative skewed delay paths and normal delay paths.

5. The unified serial link system of claim 4 wherein the voltage control oscillator further comprises a plurality of tunable delay cells, said delay cells configured to have a tunable delay of from about 80 ps to about 125 ps.

6. The unified serial link system of claim 1 wherein the phase buffer circuit is a latch buffer configured with positive feedback through cross-coupled n-channel devices.

7. The unified serial link system of claim 1 wherein the phase buffer circuit comprises a pair of inverters.

8. The unified serial link system of claim 2 wherein the multi-pole filter further comprises a ripple capacitor configured to attenuate charge pump ripple and a loop filter capacitor configured to stabilize the charge pump output and set a dominant pole.

9. The unified serial link system of claim 6 wherein the latch buffer comprises at least one CMOS, positive edge triggered latch circuit sampling latch.

10. A method for providing a unified serial link comprising the steps of:

a. providing a phase locked loop control circuit;

b. the phase locked loop control circuit generating a clock phase;

c. connecting a phase rotator circuit to the phase locked loop control circuit;

d. the phase rotator circuit receiving the clock phase from the phase locked loop control circuit;

e. the phase rotator circuit modulo shifting the clock phase into a desired phase angle;

f. connecting a phase buffer circuit to the phase rotator circuit; and

g. the phase buffer circuit buffering the phase angle to an equalization driver.

11. The method for providing a unified serial link of claim 10 further comprising the steps of:

a. providing a voltage control oscillator connected to the phase rotator circuit;

b. providing a fine control voltage signal input to the voltage control oscillator;

c. the voltage control oscillator generating the clock phase to the phase rotator and a voltage control oscillator signal;

d. providing a frequency divider connected to the voltage control oscillator;

e. the frequency divider receiving the voltage control oscillator signal;

f. the frequency divider generating a frequency divider output;

g. providing a phase-frequency detector connected to the frequency divider;

h. the phase-frequency detector receiving the frequency divider output and generating a phase-frequency detector output;

i. providing a charge pump connected to the phase-frequency detector;

j. the charge pump receiving the phase-frequency detector output and generating a charge pump output;

k. providing a multi-pole loop filter connected to the charge pump and the voltage control oscillator;

l. the multi-pole loop filter receiving the charge pump output; and

m. the multi-pole loop filter performing the step of providing the fine control voltage signal to the voltage control oscillator.

12. The method for providing a unified serial link of claim 11 further comprising the steps of:

a. providing a voltage comparator connected to the multi-pole loop filter;

b. the voltage comparator receiving the fine control voltage signal from the loop filter;

c. providing a reference generator connected to the voltage comparator;

d. the reference generator providing a reference signal to the voltage comparator;

e. the voltage comparator generating a comparator output from the fine control voltage signal and the reference signal;

f. providing a phase locked loop control logic circuit connected to the comparator;

g. the phase locked loop control logic circuit sampling the comparator output and thereby generating a control logic output;

h. providing a digital to analog converter connected to the phase locked loop control logic circuit;

i. the digital to analog converter converting the control logic output to a control voltage output;

j. providing a low pass filter connected to the digital to analog converter and to the voltage control oscillator;

k. the low pass filter receiving the control voltage output and generating a coarse control voltage signal; and

l. the voltage control oscillator receiving the coarse control voltage signal.

13. The method for providing a unified serial link of claim 11 wherein the voltage control oscillator is a dual-delay voltage controlled oscillator comprising negative skewed delay paths and normal delay paths.

14. The method for providing a unified serial link of claim 13 further comprising the steps of:

a. providing a plurality of tunable delay cells within the voltage control oscillator; and

b. tuning the delay cells to have a delay of from about 80 ps to about 125 ps.

15. The method for providing a unified serial link of claim 10 wherein the step of providing a phase buffer circuit comprises providing a latch buffer configured with positive feedback through cross-coupled n-channel devices.

16. The method for providing a unified serial link of claim 10 wherein the step of providing a phase buffer circuit comprises providing a pair of inverters.

17. The method for providing a unified serial link of claim 11 wherein the step of providing a multi-pole filter further comprises the steps of:

a. providing a ripple capacitor;

b. the ripple capacitor attenuating charge pump ripple;

c. providing a loop filter capacitor; and

d. the loop filter capacitor stabilizing the charge pump output and setting a dominant pole.

18. The method for providing a unified serial link of claim 15 further comprising the step of providing at least one CMOS, positive edge triggered latch circuit sampling latch within the latch buffer.